REMARKS

Summary of the Amendment

The specification has been amended to make minor editorial changes. Claims 1,4 and 14 have been amended.

Summary of the Official Action

In the instant Office Action, the Examiner rejected claims 1-4, 14 and 17 under 35 U.S.C.102(b) as being anticipated by Feng et al. (patent No. 5,081,563). Additionally claims 5-13, 15-16 and 18-20 were rejected under 35 U.S.C. 103(a) as being unpatentable over Feng et al. in view of Marcinkiewicz et al (patent No. 5,241,456) and Degani (patent No. 5,646,828).

It is initially noted that the obviousness rejection is not understood. While the caption in the rejection uses Marcinkiewicz and Degani as secondary references, the body of the rejection uses only one or the other of these secondary references relative to different sets of claims. Furthermore, none of the references used in rejecting the claims were cited on form PTO-892.

REQUEST FOR RECONSIDERATION

By the present amendment and remarks, Applicant submits that the rejection has been rendered moot, and respectfully requests reconsideration of the outstanding Office Action and allowance of the present application.

The subject matter of the '563 patent to Feng et al. is directed to a multi-layer "package" incorporating recessed cavities for semiconductor chips. A final product, fabricated according to the reference, is an electronic component package with multiple chips. However, the present invention is drawn to a functional printed circuit board (PCB). The functional PCB can be a small system and has a specific function.

With reference to Fig. 4 in the '563 patent, Feng disclosed a multi-layer ceramic or glass-ceramic substrate (10) with embedded conductive signal layers (16,18,and 20) and chips (56). The primary function of the substrate (10) is to provide an electrical connection among the chips (16), conductive signal layers (16, 18 and 20) and interconnection layers (62). To accomplish precise interconnection in the substrate (10), complicated fabrication processes of the conductive signal layers (16, 18 and 20) in the substrate (10) is required. Since the substrate (10) has multiple conductive signal layers, the total thickness of the substrate (10) increases with the number of layers and inhibits minimization of the package size.

With regards to the frame (10) of the present application, the frame (10) is only a supporting member to hold an embedded chip (20). Except for the conductive vias defined through the substrate, no conductive wires or layers are formed in the substrate (10) so the thickness of the functional PCB can be made as thin as possible.

Instead of using internal conductive wires or layers, in the present application, printed circuits (12)(18) are formed on either one side or two sides of the frame (10) to connect the chip (20). More particularly, the printed circuits (12)(18), which can be thin conductive material, are formed on the surfaces of the substrate. However, in the '563 patent, no printed circuits are formed on the substrate (10). The chips (56) disclosed in the patent are interconnected through internal wires (62, 64 and 66). As shown in any figure of the patent, these internal wires (62,64 and 66) are at positions above the substrate and chips, not on the surface of the substrate. These internal wires (62, 64 and 66) are further encapsulated by insulating material (60). According to figures and specification of the patent '563, Feng disclosed an electronic component packaging, not a circuit board.

Further, in the '563 patent, the cavities (44) where the chips (56) are mounted are not formed through the substrate (10). However, as shown in all drawings of the present application, the hole (101) is defined through the frame (10). The chip (56) is held in the hole of the frame by the insulating material (111) filling the hole (101).

As discussed above, the subject matter recited in the presently amended claim 1 is different from the '563 patent. Thus, the rejection under 35 U.S.C. 102 is believed to have been rendered moot.

With regard to the obviousness rejection of claim 5-13, 15-16 and 18-20, the Examiner indicated that the '456 patent to Marcinkiewicz discloses (in Fig. 1) a

PCB module comprised of a second insulation layer, a second printed circuit and multiple vias. The '828 patent to Degani supposedly discloses that a chip has multiple solder bumps connected to the printed circuit.

With reference to Figs. 1 and 2 of Marcinkiewicz, there is disclosed a substrate (12) on which a large cavity (14) is defined to hold multiple chips (26). In this patent, the chips (26) are secured to the substrate (12) by a thermoplastic polymer adhesive layer (25) (see column 7, lines 48-56). A similar cavity (16) in the lower surface (13B) of the substrate has chips (36) disposed therein. Polymer dielectric layers (42)(52) are bonded to the upper/lower surfaces of the substrate and contact pads of the chips (26)(36). Limited by the large cavity on substrate, the chips can be only gathered together in the pre-determined position, i.e. the cavity, of the substrate. In other words, the chips can not be arbitrarily distributed at any position on the substrate depending on the fabricating requirements. Further, according to Fig. 3 of patent '456, a multi-layer structure is formed by stacking different substrates. However, the electrical connection between adjacent substrates are implemented through the conductive bumps. The gap still exists between the substrates.

However, with regard to the present invention, the through holes defined through the substrate can be configured at any positions so the chips can be distributed over the substrate depending on practical requirements. Further, each chip is held in the through hole using a compressing process by which the insulation material can fill in the through hole to secure the chip to the substrate.

As shown in Fig. 6 of the present application, a multi-layer printed circuit board (PCB) is carried out by compressing multiple layers, wherein the multiple layers are interconnected through conductive vias that are formed through each layer and properly connect printed circuits on different layers. As a whole, the multi-layer structure proposed by the present invention is a small system in the form of a PCB integrated with chips of different functions.

After carefully reviewing these two patents, it is clear that neither Marcinkiewicz nor Degani teach or disclose a frame having chip holes defined through the frame. Therefore, even combining Feng's disclosure with Marcinkiewicz's or Degani's disclosure, the subject matter recited in claims 5-13, 15-16 and 18-20 is not disclosed by any combination of the references suggested by the Examiner. Accordingly, the rejection of claims 5-13, 15-16 and 18-20 under 35 U.S.C. 103 is respectfully traversed.

CONCLUSION

In view of the foregoing, it is submitted that the rejection has been rendered moot. Accordingly, reconsideration of the outstanding Office Action and allowance of the present application and all the claims therein, i.e., claims 1-20, are respectfully requested and now believed to be appropriate.

Please charge any fees necessary for consideration of the papers filed herein and refund excess payments to Deposit Account No. 50-2929.

Should the Examiner have any questions, the undersigned may be contacted at the below-listed telephone number.

Respectfully submitted,
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January 19, 2006

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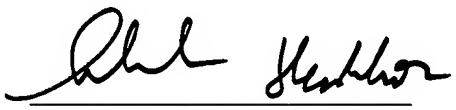

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